

ACT-SF128K16 High Speed 128Kx16 SRAM/FLASH Multichip Module



FEATURES

- 2 – 128K x 8 SRAMs & 2 – 128K x 8 Flash Die in One MCM
- Access Times of 25ns (SRAM) and 60ns (Flash) or 35ns (SRAM) and 70 or 90ns (Flash)
- 128K x 16 SRAM
- 128K x 16 5V Flash
- Organized as 128K x 16 of SRAM and 128K x 16 of Flash Memory with Separate Data Buses
- Both Blocks of Memory are User Configurable as 256K x 8
- Low Power CMOS
- Input and Output TTL Compatible Design
- MIL-PRF-38534 Compliant MCMs Available
- Decoupling Capacitors and Multiple Grounds for Low Noise
- Industrial and Military Temperature Ranges
- Industry Standard Pinouts

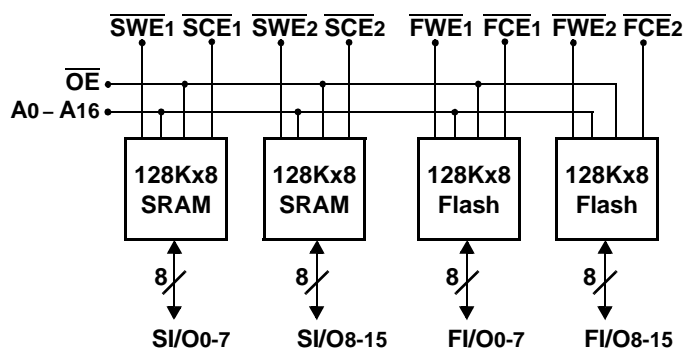
- Packaging – Hermetic Ceramic
 - 66 Pin, 1.08" x 1.08" x .160" PGA Type, No Shoulder, Aeroflex code# "P3"
 - 66 Pin, 1.08" x 1.08" x .185" PGA Type, With Shoulder, Aeroflex code# "P7"
 - 68 Lead, .94" x .94" x .140" Single-Cavity Small Outline Gull Wing, Aeroflex code# "F18" (*Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint*)
- DESC SMD Pending – 5962-96900

FLASH MEMORY FEATURES

- Sector Architecture (Each Die)
 - 8 Equal Sectors of 16K bytes each
 - Any combination of sectors can be erased with one command sequence.
- +5V Programming, 5V ±10% Supply
- Embedded Erase and Program Algorithms
- Hardware and Software Write Protection
- Internal Program Control Time.
- 10,000 Erase/Program Cycles

Note: Programming information available upon request

Block Diagram – PGA Type Package (P3,P7) and CQFP (F18)



Pin Description

FI/O0-15	Flash Data I/O
SI/O0-15	SRAM Data I/O
A0-16	Address Inputs
$\overline{FWE}1-2$	Flash Write Enables
$\overline{SWE}1-2$	SRAM Write Enables
$\overline{FCE}1-2$	Flash Chip Enables
$\overline{SCE}1-2$	SRAM Chip Enables
\overline{OE}	Output Enable
NC	Not Connected
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Case Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Parameter	
Flash Data Retention	10 Years
Flash Endurance (Write/Erase Cycles)	10,000

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Capacitance

($V_{IN} = 0V$, $f = 1MHz$, $T_C = 25°C$)

Symbol	Parameter	Maximum	Units
C_{AD}	$A_0 - A_{16}$ Capacitance	50	pF
C_{OE}	\overline{OE} Capacitance	50	pF
F/S $C_{WE1,2}$	F/S Write Enable Capacitance	20	pF
F/S $C_{CE1,2}$	F/S Chip Enable Capacitance	20	pF
F/S $C_{I/O}$	I/O ₀ – I/O ₁₅ Capacitance	20	pF

These parameters are guaranteed by design but not tested

DC Characteristics

($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_C = -55°C$ to $+125°C$, unless otherwise indicated)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	$V_{CC} = Max$, $V_{IN} = 0$ to V_{CC}		10	μA
Output Leakage Current	I_{LO}	$\overline{FCE} = \overline{SCE} = V_{IH}$, $\overline{OE} = V_{IH}$, $V_{OUT} = 0$ to V_{CC}		10	μA
SRAM Operating Supply Current x 16 Mode	I_{CCx16}	$\overline{SCE} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 5MHz$, $V_{CC} = Max$, $\overline{FCE} = V_{IH}$		250	mA
Standby Current	I_{SB}	$\overline{FCE} = \overline{SCE} = V_{IH}$, $\overline{OE} = V_{IH}$, $f = 5MHz$, $V_{CC} = Max$		40	mA
SRAM Output Low Voltage	V_{OL}	$I_{OL} = 8 mA$, $V_{CC} = 4.5V$		0.4	V
SRAM Output High Voltage	V_{OH}	$I_{OH} = -4.0 mA$, $V_{CC} = 4.5V$	2.4		V
Flash Vcc Active Current for Read (1)	I_{CC1}	$\overline{FCE} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{SCE} = V_{IH}$		100	mA
Flash Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{FCE} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{SCE} = V_{IH}$		130	mA
Flash Output Low Voltage	V_{OL}	$I_{OL} = 12 mA$, $V_{CC} = 4.5V$, $\overline{SCE} = V_{IH}$		0.45	V
Flash Output High Voltage	V_{OH}	$I_{OH} = -2.5 mA$, $V_{CC} = 4.5V$, $\overline{SCE} = V_{IH}$	$0.85 \times V_{CC}$		V
Flash Low Vcc Lock Out Voltage	V_{LKO}		3.2		V

Notes: 1) The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5MHz). The frequency component typically is less than 2mA/MHz, with \overline{OE} at V_{IH} 2) I_{CC} active while Embedded Algorithm (program or erase) is in progress 3) DC test conditions: $V_{IL} = 0.3V$, $V_{IH} = V_{CC} - 0.3V$

SRAM AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Symbol	-025		-035		Units
		Min	Max	Min	Max	
Read Cycle Time	t _{RC}	25		35		ns
Address Access Time	t _{AA}		25		35	ns
Chip Select Access Time	t _{ACE}		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		ns
Output Enable to Output Valid	t _{OE}		15		20	ns
Chip Select to Output in Low Z *	t _{CLZ}	3		3		ns
Output Enable to Output in Low Z *	t _{OLZ}	0		0		ns
Chip Deselect to Output in High Z *	t _{CHZ}		12		20	ns
Output Disable to Output in High Z *	t _{OHZ}		12		20	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Symbol	-025		-035		Units
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	25		35		ns
Chip Select to End of Write	t _{CW}	20		25		ns
Address Valid to End of Write	t _{AW}	20		25		ns
Data Valid to End of Write	t _{DW}	15		20		ns
Write Pulse Width	t _{WP}	20		25		ns
Address Setup Time	t _{AS}	0		0		ns
Output Active from End of Write *	t _{OW}	0		0		ns
Write to Output in High Z *	t _{WHZ}		10		20	ns
Data Hold from Write Time	t _{DH}	0		0		ns
Address Hold Time	t _{AH}	0		0		ns

* Parameters guaranteed by design but not tested

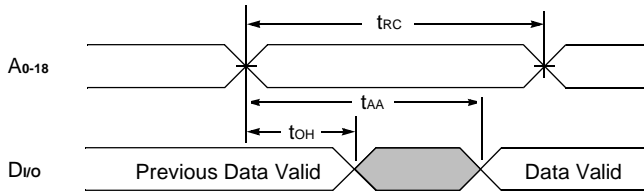
SRAM Truth Table

Mode	SCE	OE	SWE	Data I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active
Write	L	X	L	Data In	Active

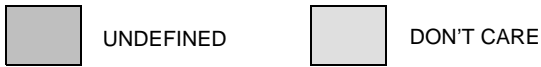
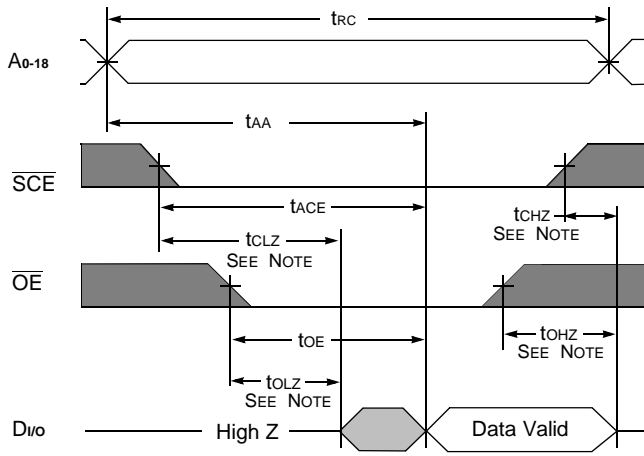
Timing Diagrams — SRAM

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{SCE} = \overline{OE} = V_{IL}, \overline{SWE} = V_{IH}$)

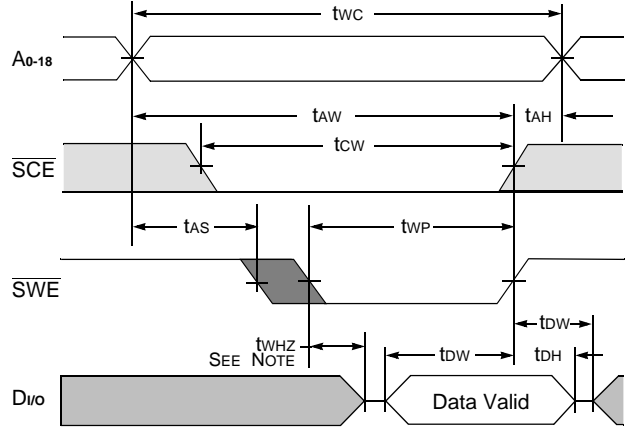


Read Cycle 2 ($\overline{SWE} = V_{IH}$)

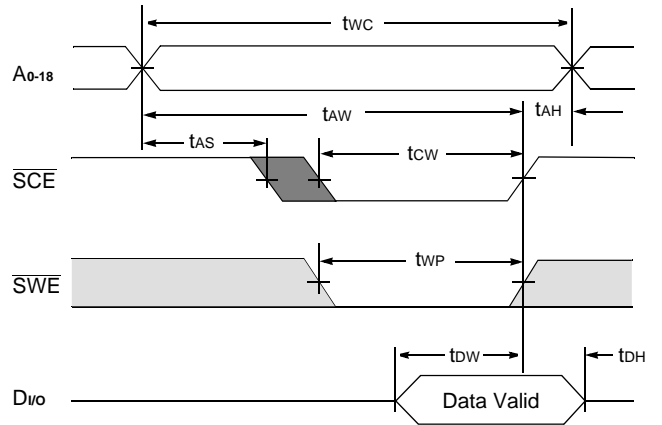


Write Cycle Timing Diagrams

Write Cycle (\overline{SWE} Controlled, $\overline{OE} = V_{IH}$)

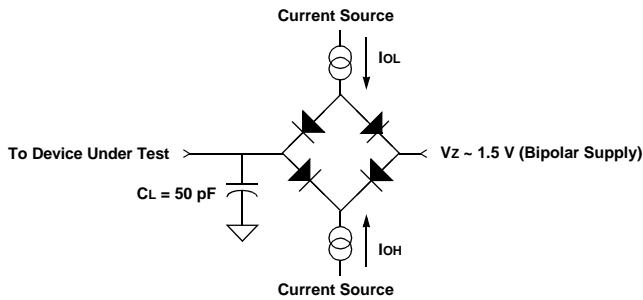


Write Cycle (\overline{SCE} Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Notes:

- 1) V_Z is programmable from -2V to +7V. 2) I_{oL} and I_{oH} programmable from 0 to 16 mA. 3) Tester Impedance $Z_o = 75\Omega$. 4) V_Z is typically the midpoint of V_{oH} and V_{oL} . 5) I_{oL} and I_{oH} are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

AC Test Conditions

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Flash AC Characteristics – Read Only Operations

(V_{cc} = 5.0V, V_{ss} = 0V, T_c = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	60		70		90		ns
Address Access Time	t _{AVQV}	t _{ACC}		60		70		90	ns
Chip Enable Access Time	t _{ELQV}	t _{CE}		60		70		90	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		30		35		40	ns
Chip Enable to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		25	ns
Output Enable High to Output High Z(1)	t _{GHQZ}	t _{DF}		20		20		25	ns
Output Hold from Address, CE or OE Change, Whichever is First	t _{AXQX}	t _{OH}	0		0		0		ns

Note 1. Guaranteed by design, but not tested

Flash AC Characteristics – Write/Erase/Program Operations, FWE Controlled

(V_{cc} = 5.0V, V_{ss} = 0V, T_c = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAC}	t _{WC}	60		70		90		ns
Chip Enable Setup Time	t _{ELWL}	t _{CE}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	30		35		45		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	30		30		45		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		45		45		ns
Chip Enable Hold Time	t _{WHEH}	t _{CH}	0		0		0		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		ns
Duration of Byte Programming Operation	t _{WHWH1}		14	TYP	14	TYP	14	TYP	μs
Sector Erase Time	t _{WHWH2}			60		60		60	Sec
Chip Erase Time	t _{WHWH3}			120		120		120	Sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μs
V _{cc} Setup Time		t _{VCE}	50		50		50		μs
Output Enable Setup Time		t _{OES}		12.5		12.5		12.5	Sec
Output Enable Hold Time ¹		t _{OEH}	10		10		10		ns

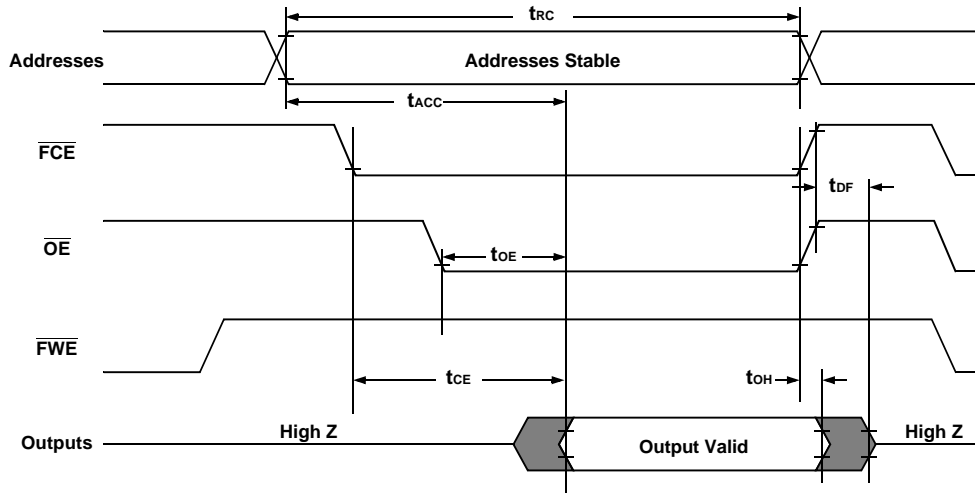
Note: 1. For Toggle and Data Polling.

Flash AC Characteristics – Write/Erase/Program Operations, FCE Controlled

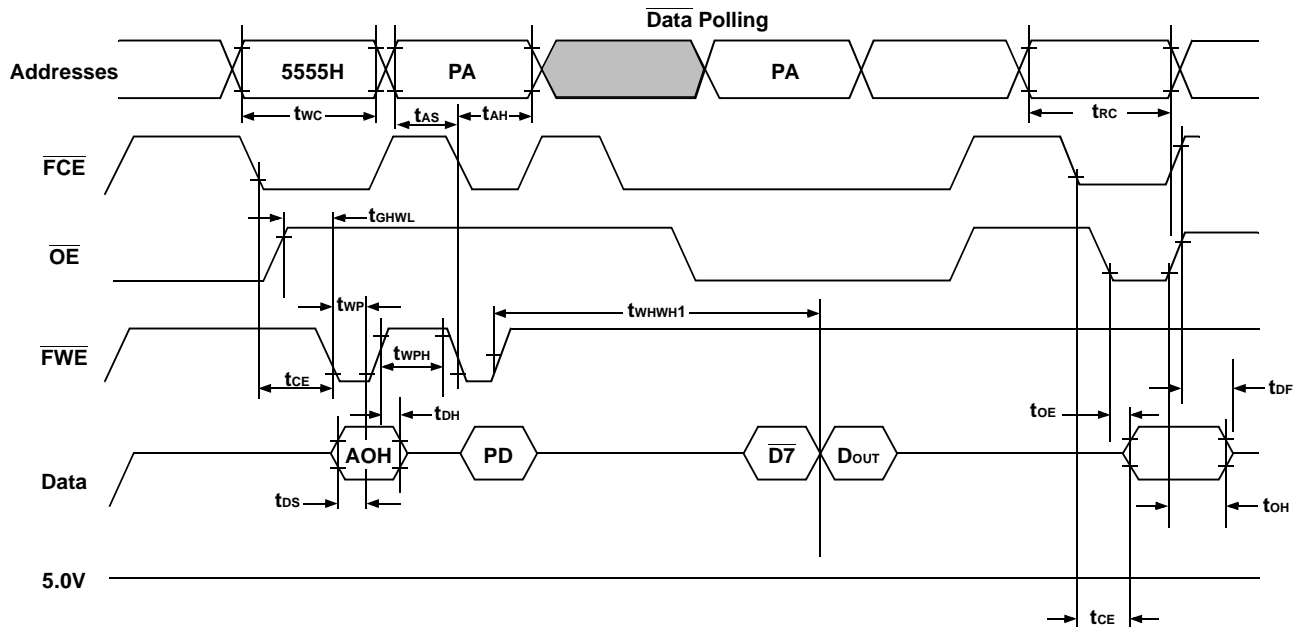
(V_{cc} = 5.0V, V_{ss} = 0V, T_c = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAC}	t _{WC}	60		70		90		ns
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		ns
Chip Enable Pulse Width	t _{ELEH}	t _{CP}	35		35		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	30		30		50		ns
Data Hold Time	t _{EHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	45		45		50		ns
Write Enable Hold from Write Enable High	t _{EHWH}	t _{WH}	0		0		0		ns
Chip Enable Pulse Width High	t _{EHEL}	t _{CPH}	20		20		20		ns
Duration of Byte Programming	t _{WHWH1}		14	TYP	14	TYP	14	TYP	μs
Sector Erase Time	t _{WHWH2}			60		60		60	Sec
Chip Erase Time	t _{WHWH3}			120		120		120	Sec
Read Recovery Time	t _{GHEL}		0		0		0		ns
Chip Programming Time				12.5		12.5		12.5	Sec

AC Waveforms for Flash Memory Read Operations

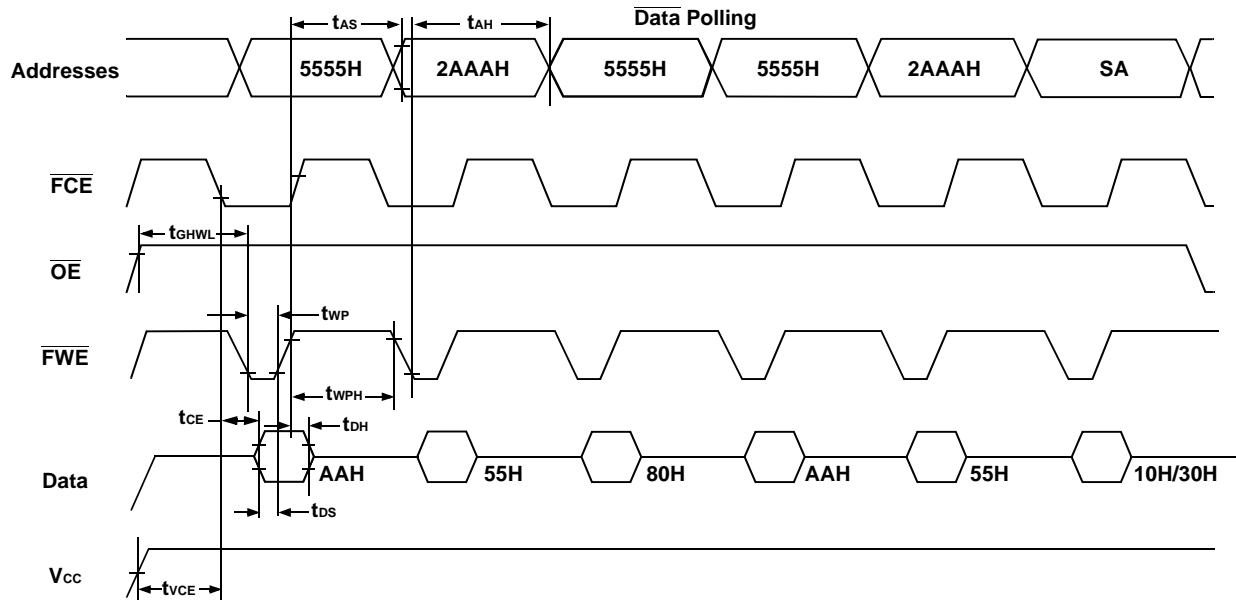


Write/Erase/Program Operation for Flash Memory, \overline{FWE} Controlled



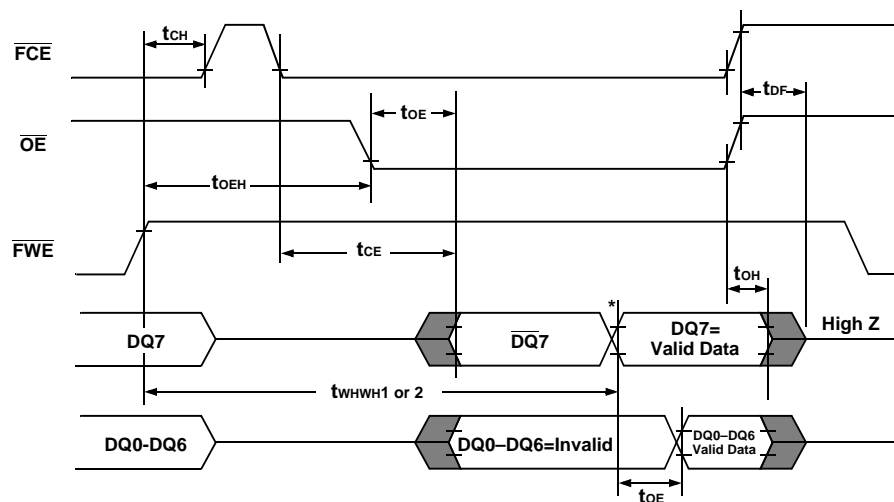
- Notes:**
1. PA is the address of the memory location to be programmed.
 2. PD is the data to be programmed at byte address.
 3. D7 is the Output of the complement of the data written to the device.
 4. Dout is the output of the data written to the device.
 5. Figure indicates last two bus cycles of four bus cycle sequence.

AC Waveforms Chip/Sector Erase Operations for Flash Memory



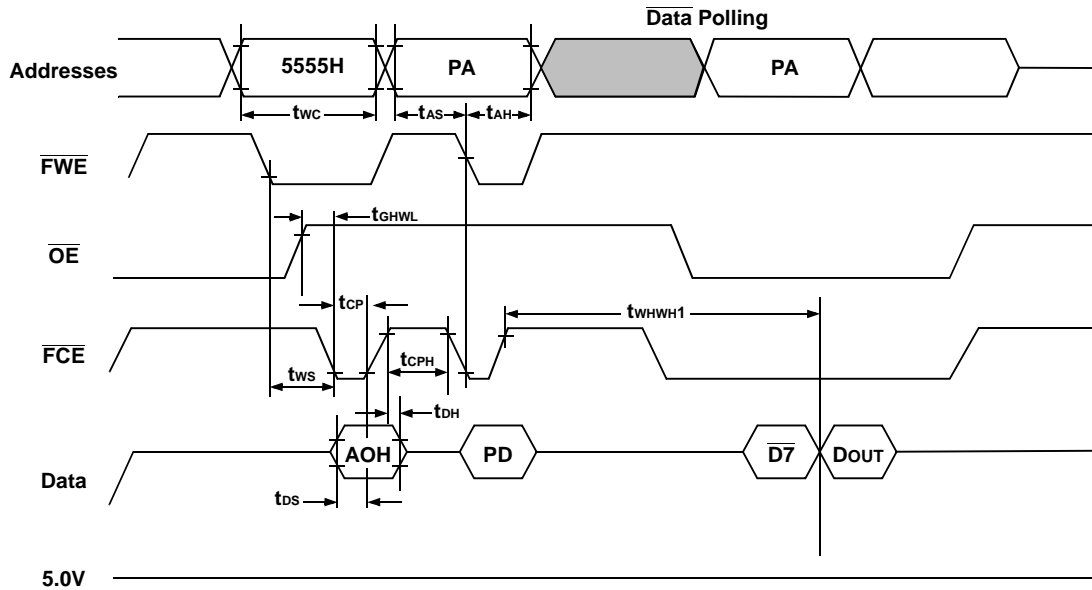
- Notes:**
1. SA is the sector address for sector erase.

AC Waveforms for Data Polling During Embedded Algorithm Operations for Flash Memory



* DQ7=Valid Data (The device has completed the Embedded operation).

Write/Erase/Program Operation for Flash Memory, $\overline{\text{FCE}}$ Controlled



Notes:

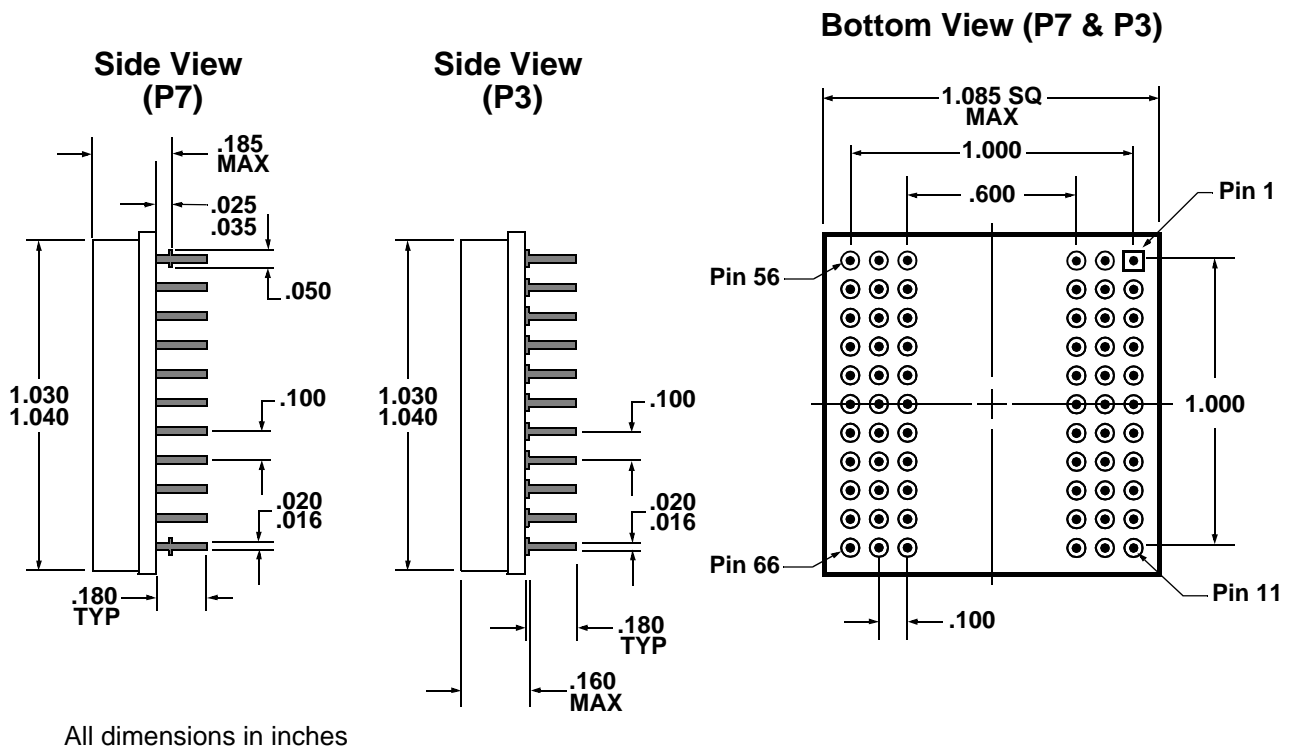
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{\text{D7}}$ is the Output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	SI/O ₈	18	A ₁₂	35	FI/O ₉	52	$\overline{\text{FWE}}_1$
2	SI/O ₉	19	V _{cc}	36	FI/O ₁₀	53	$\overline{\text{FCE}}_1$
3	SI/O ₁₀	20	$\overline{\text{SCE}}_1$	37	A ₆	54	GND
4	A ₁₃	21	NC	38	A ₇	55	FI/O ₃
5	A ₁₄	22	SI/O ₃	39	NC	56	FI/O ₁₅
6	A ₁₅	23	SI/O ₁₅	40	A ₈	57	FI/O ₁₄
7	A ₁₆	24	SI/O ₁₄	41	A ₉	58	FI/O ₁₃
8	NC	25	SI/O ₁₃	42	FI/O ₀	59	FI/O ₁₂
9	SI/O ₀	26	SI/O ₁₂	43	FI/O ₁	60	A ₀
10	SI/O ₁	27	$\overline{\text{OE}}$	44	FI/O ₂	61	A ₁
11	SI/O ₂	28	NC	45	V _{cc}	62	A ₂
12	$\overline{\text{SWE}}_2$	29	$\overline{\text{SWE}}_1$	46	$\overline{\text{FCE}}_2$	63	FI/O ₇
13	$\overline{\text{SCE}}_2$	30	SI/O ₇	47	$\overline{\text{FWE}}_2$	64	FI/O ₆
14	GND	31	SI/O ₆	48	FI/O ₁₁	65	FI/O ₅
15	SI/O ₁₁	32	SI/O ₅	49	A ₃	66	FI/O ₄
16	A ₁₀	33	SI/O ₄	50	A ₄		
17	A ₁₁	34	FI/O ₈	51	A ₅		

"P3" — 1.08" SQ PGA Type (without shoulder) Package

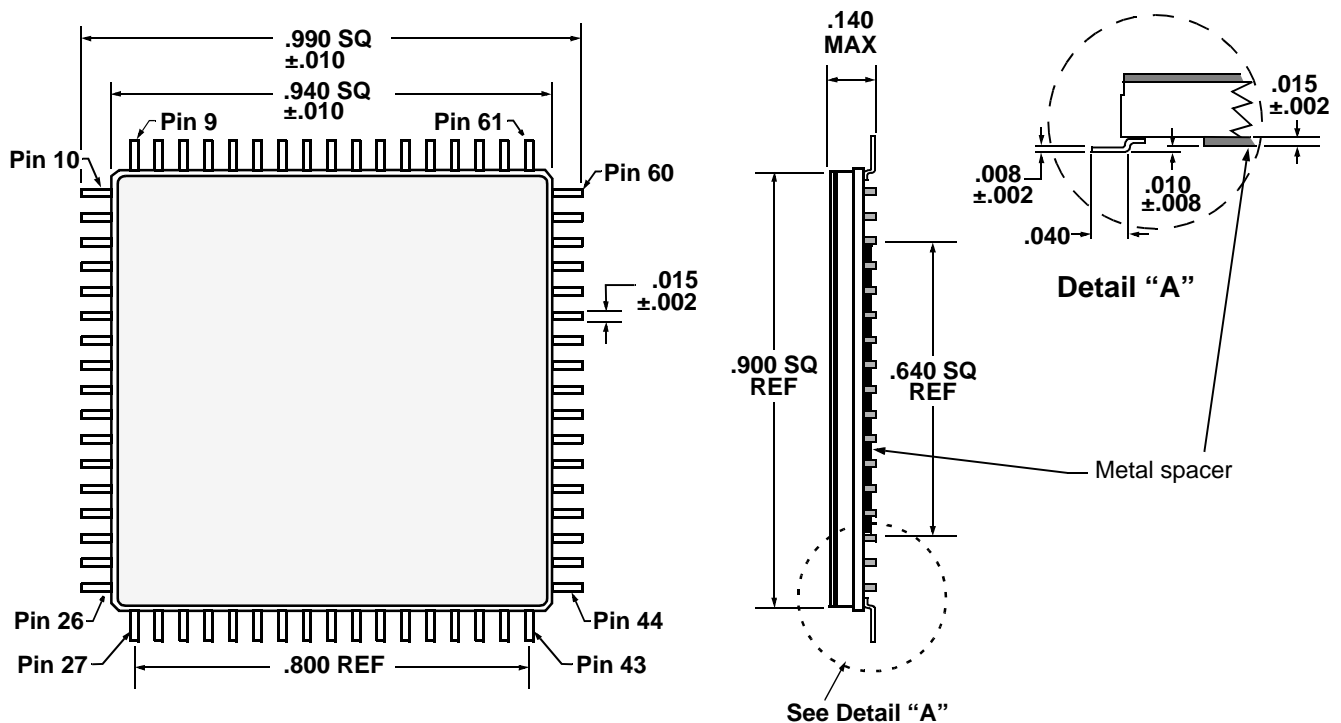
"P7" — 1.08" SQ PGA Type (with shoulder) Package



Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	\overline{OE}	52	GND
2	\overline{FCE}_1	19	SI/O ₈	36	\overline{SCE}_2	53	FI/O ₇
3	A ₅	20	SI/O ₉	37	NC	54	FI/O ₆
4	A ₄	21	SI/O ₁₀	38	\overline{SWE}_2	55	FI/O ₅
5	A ₃	22	SI/O ₁₁	39	\overline{FWE}_1	56	FI/O ₄
6	A ₂	23	SI/O ₁₂	40	\overline{FWE}_2	57	FI/O ₃
7	A ₁	24	SI/O ₁₃	41	NC	58	FI/O ₂
8	A ₀	25	SI/O ₁₄	42	NC	59	FI/O ₁
9	NC	26	SI/O ₁₅	43	NC	60	FI/O ₀
10	SI/O ₀	27	V _{CC}	44	FI/O ₁₅	61	V _{CC}
11	SI/O ₁	28	A ₁₁	45	FI/O ₁₄	62	A ₁₀
12	SI/O ₂	29	A ₁₂	46	FI/O ₁₃	63	A ₉
13	SI/O ₃	30	A ₁₃	47	FI/O ₁₂	64	A ₈
14	SI/O ₄	31	A ₁₄	48	FI/O ₁₁	65	A ₇
15	SI/O ₅	32	A ₁₅	49	FI/O ₁₀	66	A ₆
16	SI/O ₆	33	A ₁₆	50	FI/O ₉	67	\overline{SWE}_1
17	SI/O ₇	34	\overline{SCE}_1	51	FI/O ₈	68	\overline{FCE}_2

"F18" — CQFP Package



All dimensions in inches

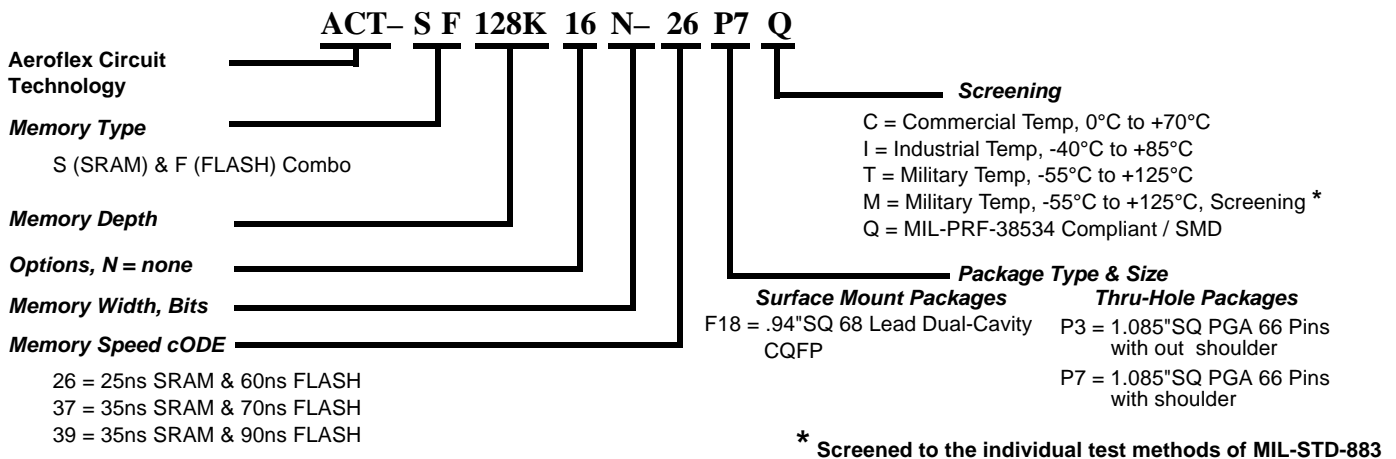


Ordering Information

Model Number	DESC SMD Number	Speed	Package
ACT-SF128K16N-26P3Q	5462-96900*	25(S) / 60(F) ns	1.08"SQ PGA-Type
ACT-SF128K16N-37P3Q	5462-96900*	35(S) / 70(F) ns	1.08"SQ PGA-Type
ACT-SF128K16N-39P3Q	5462-96900*	35(S) / 90(F) ns	1.08"SQ PGA-Type
ACT-SF128K16N-26P7Q	5462-96900*	25(S) / 60(F) ns	1.08"SQ PGA-Type
ACT-SF128K16N-37P7Q	5462-96900*	35(S) / 70(F) ns	1.08"SQ PGA-Type
ACT-SF128K16N-39P7Q	5462-96900*	35(S) / 90(F) ns	1.08"SQ PGA-Type
ACT-SF128K16N-26F18Q	5462-96900*	25(S) / 60(F) ns	.94"sq CQFP
ACT-SF128K16N-37F18Q	5462-96900*	35(S) / 70(F) ns	.94"sq CQFP
ACT-SF128K16N-39F18Q	5462-96900*	35(S) / 90(F) ns	.94"sq CQFP

Note: (S) = Speed for SRAM, (F) = Speed for FLASH
 * Pending

Part Number Breakdown



Specification subject to change without notice

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